## CLAIMS

What is claimed is:

1. A method comprising:

forming a via layer on a semiconductor device substrate;

forming a trench layer on the via dielectric layer;

forming a trench through the trench layer to expose the via layer;

forming a via in the via layer in the trench to expose the substrate; and

forming a semiconductor material in the via and in the trench.

2. The method of claim 1, wherein forming a via layer comprises:

forming a primary dielectric layer comprising a material having a first etch characteristic; and

forming a secondary dielectric layer on the primary layer, the secondary dielectric layer comprising a material having a second etch characteristic different from the first etch characteristic.

3. The method of claim 2, wherein the primary dielectric layer comprises silicon dioxide and the secondary dielectric layer comprises silicon nitride.

4. The method of claim 2, wherein the substrate comprises a first semiconductor material and a second semiconductor material on a portion of the first semiconductor material, the second semiconductor material having a different lattice parameter than the first semiconductor material and forming a via layer comprises forming a via layer to a thickness to minimize a crystalline defect in the second semiconductor material from propagating beyond a depth of the via.

5. The method of claim 1, further comprising:

planarizing an exposed surface of the semiconductor material in the trench.

6. The method of claim 5, wherein planarizing comprises planarizing of the semiconductor material in the trench to a thickness suitable as a device channel.

7. The method of claim 1, further comprising electrically isolating a portion of the semiconductor material formed in the trench from a portion of the semiconductor material formed in the via.

8. The method of claim 7, wherein the isolated portion of the semiconductor material formed in the trench has a dimension suitable as a circuit device base.

9. The method of claim 1, wherein forming a trench layer comprises:

forming a primary dielectric layer comprising a material having a first etch characteristic different than a portion of the via layer; and

forming a secondary dielectric layer comprising a material having a second etch characteristic different than the primary dielectric layer.

10. The method of claim 9, wherein forming the primary dielectric layer comprises forming a layer to a thickness selected to be suitable as a circuit device base.

11. The method of claim 1, further comprising removing the trench layer after forming a semiconductor material in the trench.

12. The method of claim 1, further comprising crystallizing the semiconductor material in the trench.

13. The method of claim 12, wherein crystallizing comprises annealing the semiconductor material at a temperature suitable to produce a single crystal mass.

14. The method of claim 1, wherein forming a trench layer comprises:

forming a trench of a length at least suitable for a device channel; and

forming a trench pad having dimensions different than the trench adjacent to the trench,

wherein forming a via comprises forming a via in a portion of the trench pad.

15. A method comprising:

forming a first dielectric layer on a device substrate;

forming a second dielectric layer on the first dielectric layer, the second dielectric layer comprising a material having an etch characteristic different than a material of the first dielectric layer;

forming a third dielectric layer on the second dielectric layer, the third dielectric layer comprising a material having an etch characteristic different than the material of the second dielectric layer;

forming a fourth dielectric layer on the third dielectric layer, the fourth dielectric layer comprising a material having an etch characteristic different than a material of the third-dielectric layer;

forming a trench through the third dielectric layer;

forming a via in the trench to expose the substrate; and

forming a semiconductor material in the via and in the trench.

16. The method of claim 15, further comprising crystallizing the semiconductor material in the trench.

17. The method of claim 15, further comprising:

planarizing an exposed surface of the semiconductor material in the trench.

18. The method of claim 17, wherein planarizing comprises planarizing of the semiconductor material in the trench to a thickness suitable as a device channel.

19. The method of claim 15, further comprising removing the third dielectric layer and the fourth dielectric layer after forming a semiconductor material in the trench.

20. The method of claim 19, further comprising electrically isolating a portion of the semiconductor material formed in the trench from a portion of the semiconductor material formed in the via.

21. The method of claim 20, wherein the isolated portion of the semiconductor material formed in the trench has a dimension suitable as a circuit device base.

22. The method of claim 15, wherein each of the dielectric layers comprises a dielectric material, the first dielectric layer and the third dielectric layer comprise similar materials, and the second dielectric layer and the fourth dielectric layer comprise similar materials.

23. The method of claim 15, wherein the substrate comprises a first semiconductor material and a second semiconductor material on the first semiconductor material, the second semiconductor material having a different lattice structure than the first semiconductor material and forming a first dielectric layer comprises forming a first dielectric layer to a thickness to minimize a crystalline defect in the second semiconductor material from propagating beyond a depth of the via.

24. The method of claim 15, wherein forming a trench layer comprises:

forming a trench of a length at least suitable for a device channel; and

forming a trench pad having a dimension different than the trench adjacent to the trench,

wherein forming a via comprises forming a via in a portion of the trench pad.

25. An apparatus comprising:

a device substrate;

a dielectric layer formed on a surface of the device substrate; and

a device base formed on the dielectric layer comprising a crystalline structure derived from the device substrate.

26. The apparatus of claim 25, wherein the device substrate comprises a first semiconductor material and a second semiconductor material formed on the first semiconductor material and defining the surface of the device substrate, the second semiconductor material comprising a different lattice structure than the first semiconductor material.

27. The apparatus of claim 26, wherein the first semiconductor material and the second semiconductor material each have a carrier mobility property, and the second semiconductor material has a greater mobility than the first semiconductor material.